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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,704	EHMANN ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-17,19-25,27,28 are rejected under 35 U.S.C. 102(a) as being anticipated by Swanson et al. (USPN 6292911B1). As appears in claim 1, Swanson et al. discloses a data-generation circuit adapted to provide a first data stream in column 6, lines 43-52; a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior-in-time in column 6, lines 20-25; state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path in column 6, line 66 – column 7, line 15; and a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality in column 7, lines 44-55.

3. As per claim 2, Swanson et al. discloses wherein the state machine circuitry includes a command state machine and a bus master state machine, the command

state machine being coupled to the memory arrangement and data-generation circuit, and adapted to direct the bus master state machine to assemble portions of the first data stream into test-traffic having pre-defined type, pattern and behavior-in-time responsive to the programmable commands, and the bus master state machine is coupled to the digital data path and adapted to communicate the test-traffic onto the digital data path responsive to the command state machine in column 6, line 66 – column 7, line 15; and column 7, lines 26-43.

4. As per claim 3, Swanson et al. discloses wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of 1, 2, 4, 8, 16, 32, and 64 words per burst in column 7, lines 1-15.

5. As per claim 4, Swanson et al. discloses wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of other than 1, 2, 4, 8, 16, 32, and 64 transfers per burst in column 7, lines 1-15.

6. As per claim 5, Swanson et al. discloses wherein the state machine circuitry is further adapted to receive the first data stream from the data-generation circuit without generating test-traffic on the digital data path in column 6, line 66 – column 7, line 15.

7. As per claim 6, Swanson et al. discloses wherein the state machine circuitry is adapted to pause in response to programmable commands in column 7, lines 16-25.

8. As per claim 7, Swanson et al. discloses a bus interface circuit coupled between the memory arrangement and the digital data path, the bus interface circuit adapted to

pass programmable commands received via the digital data path to the memory arrangement in column 7, lines 26-43.

9. As per claim 8, Swanson et al. discloses wherein the first data stream is a repeatable sequence of binary data in column 6, line 66 – column 7, line 15.

10. As per claim 9, Swanson et al. discloses the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement in column 7, lines 44-55.

11. As per claim 10, Swanson et al. discloses wherein the first data stream comprises a sequence of pseudo-random numbers in column 6, line 66 – column 7, line 15.

12. As per claim 11, Swanson et al. discloses wherein the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement in column 7, lines 44-55.

13. As per claim 12, Swanson et al. discloses wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream comprising a sequence of LFSR values in column 6, lines 41-52.

14. As per claim 13, Swanson et al. discloses wherein the state machine circuitry is configured and arranged to seed the LFSR and control content of the first data stream in column 6, line 66 – column 7, line 15.

15. As per claim 14, Swanson et al. discloses wherein the status and feedback circuit is further adapted to verify monitored test-traffic against corresponding LFSR values,

and the feedback signal being an interrupt generated indicative of the test-traffic verification in column 7, lines 44-55.

16. As per claim 15, Swanson et al. discloses wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal being an interrupt generated indicative of the test-traffic verification in column 7, lines 44-64.

17. As per claim 16, Swanson et al. discloses wherein the memory arrangement includes command registers adapted to store programmable commands, configuration registers adapted to store traffic generation process control information and status registers adapted to store test-traffic verification information in column 6, lines 20-25.

18. As per claim 17, Swanson et al. discloses wherein the status and feedback circuit includes a counter adapted to specify a number of command repetitions, and a loop timer adapted to specify a period within which a set of programmable commands must execute in column 5, lines 38-50 and column 8, lines 14-30.

19. As per claim 19, Swanson et al. discloses a digital data path in column 4, lines 34-45; a plurality of traffic sources, each traffic source coupled to the digital data path and adapted to communicate non-test-traffic onto the digital data path in column 4, lines 18-23; and a circuit arrangement for generating test-traffic coupled to the digital data path, the circuit arrangement including, a data-generation circuit adapted to provide a first data stream in column 6, lines 43-52; a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior-in-time in column 6, lines 20-25; state

machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path in column 6, line 66 – column 7, line 15; and a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality, wherein at least one of the plurality of traffic sources is a processor circuit in column 7, lines 44-55.

20. As per claim 20, Swanson et al. discloses wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream consists of a sequence of pseudo-randomly generated binary numbers representing LFSR values in column 6, lines 41-52.

21. As per claim 21, Swanson et al. discloses wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal is an interrupt generated indicative of the test-traffic verification in column 7, lines 44-64.

22. As per claims 22 and 28, Swanson et al. discloses coupling a dedicated test-traffic source to the digital data path in column 4, lines 18-23; providing a first data stream, the first data stream being replicatable in column 6, lines 43-52; storing a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior in column 6, lines 20-25; assembling

portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands in column 6, line 66 – column 7, line 15; generating test-traffic on the digital data path; monitoring the digital data path for the test-traffic; verifying the monitored test-traffic against a corresponding first data stream; and generating a feedback signal indicative of the test-traffic verification in column 7, line 44-55.

23. As per claim 23, Swanson et al. discloses wherein the first data stream is a sequence of pseudo-random numbers each representative of a linear feedback shift register (LFSR) value in column 6, lines 41-52.

24. As per claim 24, Swanson et al. discloses verifying monitored test-traffic against a corresponding LFSR value, wherein the feedback signal is an interrupt indicative of each test-traffic verification in column 6, lines 41-52.

25. As per claim 25, Swanson et al. disclose counting a predetermined number of command-execution repetitions; timing each command-execution repetition against an associated programmable period; and generating a feedback signal indicative of a command-execution repetition exceeding the associated programmable period in column 5, lines 38-50 and column 8, lines 14-30.

26. As per claim 27, Swanson et al. discloses wherein test-traffic type is one of a group consisting of 1, 2, 4, 8, 16, 32, and 64 transfers per burst in column 7, lines 1-15.

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 18 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Swanson et al. in view of Kim et al. (US Publication Number 20020138678A1). Swanson et al. fails to explicitly state the digital data path is an AHB protocol bus.

Kim et al. discloses this limitation on page 4, paragraph 0075, "System 400 includes a system bus 410 that can be an advanced microcontroller bus architecture (AMBA) bus developed, for example, by Advance RISC Machines (ARM) Co. System bus 410 can be made by a advanced high performance bus (AHB)."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the digital data path be an AHB protocol bus. A person of ordinary skill in the art would have been motivated to have the digital data path be an AHB protocol bus because the AHB bus allows the transfer of data from one device to another. Kim et al. discloses this on page 6, paragraph 0111.

Response to Arguments

29. Applicant's arguments filed 02/14/2005 have been fully considered and have been found to not be persuasive.

Applicant argues on page 8, under the Remarks Section, "Applicant therefore fails to recognize how the Office Action is asserting the '911 teachings as corresponding to Applicant's claimed invention. As a specific example, the Office Action cites col. 5, lines 38-50, as disclosing the claimed memory arrangement adapted to buffer a plurality of programmable commands that are indicative of at least one of test-traffic type,

pattern, and behavior-in-time. The discussion at column 5 does not refer to a memory arrangement nor does the cited portion discuss the apparent memory circuit of the corresponding figure 1, memory 24. Moreover, Applicant fails to recognize any teachings in the '911 reference of programmable commands that are indicative of specific test-traffic parameters, as discussed at page 7 of the instant Specification. For example, the Specification explains that 'traffic pattern' is described as a sequence of traffic generator operations, each operation typically including a direction (e.g., read or write) and an address; and 'traffic behavior-in-time' is described as a frequency of generated bus traffic with respect to time. The Office Action does not identify any commands related to data path test-traffic, as claimed and therefore, also does not identify state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern, and behavior-in-time is selected responsive to the programmable commands, as claimed."

Examiner respectfully disagrees. Examiner would like to point out that the data-generation circuit is the test circuit depicted in column 6, lines 43-52; the memory arrangement is actually disclosed in column 6, lines 20-25 as 'memory 24', the Examiner pointed out a different column and line numbers in the previous action; the programmable commands are the test bit patterns which are indicative of the pattern; the state machine circuitry is the LFSR disclosed in column 6, line 66 – column 7, line 15, which forms and generates the test data patterns; the status and feedback circuit is the circuit disclosed in column 7, lines 44-55.

Applicant also argues on page 9 of the Remarks Section, "Applicant is also confused by the Office Action's citation to col. 7, lines 44-55 as corresponding to the claimed status and feedback circuit that is adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test traffic throughput and test-traffic quality. The cited portion of the '911 reference discusses a comparison to determine the accuracy of a test pattern received by a component with respect to the test pattern that was generated and transmitted to the component. Applicant fails to recognize how the '911 comparison would correspond to the claimed digital data path monitoring."

Examiner would like to point out that the digital data path is monitored by seeing if the pattern generated by the controller sent to the RDRAM and sent back across the digital data path are the same in order to detect errors, which is disclosed in column 7, lines 44-55 and in Fig. 2. Column 2, lines 45-50 disclose that this technique is used to monitor the data channel of the invention disclosed in Swanson et al.

Applicant argues on page 9 of the Remarks Section, "Applicant traverses because the Office Action fails to present any evidence that the skilled artisan would be motivated to modify the '911 reference as asserted...The Office Action presents no evidence form the cited references that the skilled artisan would replace the '911 channel 12 with a different type of bus, or more specifically, an AHB protocol bus."

Examiner would like to point out that the reason to combine comes from the '911 reference in column 3, lines 40-41, "...the data channel 12 can be of a variety of high-speed data channels..."; therefore, the secondary reference was brought in to disclose

the AHB protocol bus and the motivation comes from page 6, paragraph 0111 to state that the AHB protocol bus is another type of bus used to transfer data from one device to another.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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